A Compact Resistor-Based CMOS Temperature Sensor With an Inaccuracy of 0.12 °C (3σ) and a Resolution FoM of 0.43 pJ·K² in 65-nm CMOS

Woojun Choi, Student Member, IEEE, Yongtae Lee, Student Member, IEEE, Seonhong Kim, Sanghoon Lee, Jieun Jang, Junhyun Chun, Kofi A. A. Makinwa, Fellow, IEEE, and Youngcheol Chae, Member, IEEE

Abstract—This paper presents a compact resistor-based CMOS temperature sensor intended for dense thermal monitoring. It is based on an RC poly-phase filter (PPF), whose temperature-dependent phase shift is read out by a frequency-locked loop (PLL). The PPF’s phase shift is determined by a zero-crossing (ZC) detector, allowing the rest of the PLL to be realized in an area-efficient manner. Implemented in a 65-nm CMOS technology, the sensor occupies only 7000 μm². It can operate from supply voltages as low as 0.85 V and consumes 68 μW. A sensor based on a PPF made from silicided p-poly resistors and metal–insulator–metal (MIM) capacitors achieves an inaccuracy of ±0.12 °C (3σ) from −40 °C to 85 °C and a resolution of 2.5 mK (rms) in a 1-ms conversion time. This corresponds to a resolution figure-of-merit (FoM) of 0.43 pJ·K².

Index Terms—Area-efficient, CMOS temperature sensor, energy-efficient, frequency-locked loop (PLL), poly-phase filter (PPF), resistor-based sensor, trimming, zero-crossing (ZC) detection.

I. INTRODUCTION

TODAY’S microprocessors and DRAMs contain billions of transistors operating at gigahertz clock speed. Since the self-heating of such large chips can severely degrade their performance, thermal management is a key design consideration [1]–[3]. On-chip temperature sensors provide local temperature information about thermal gradients and hot spots, and thus prevent overheating and enhance reliability. Since the exact location of hotspots is difficult to predict in the design phase, the sensors should be as densely distributed as possible. As a result, they must be small (<0.01 mm²), low power (<100 μW), and energy-efficient (<1 pJ·K²). They should also be moderately accurate (3σ inaccuracy < ±1 °C) to avoid the need for large guard-bands to account for sensing errors and guarantee reliability. Furthermore, since they must track fast on-chip temperature gradients, their conversion time should be about 1 ms or less.

Conventional bipolar junction transistor (BJT)-based temperature sensors are widely used for on-chip temperature sensors due to their excellent accuracy [3]–[7]. However, they are based on parasitic p-n-p or n-p-n transistors, which are increasingly difficult to realize in scaled technologies. Moreover, their base–emitter voltages (~0.7 V at room temperature) do not scale with technology, making them incompatible with the sub-1-V supply voltages common in modern CMOS processes. Although this can be circumvented by using a voltage doubler [4], the resulting accuracy (±2.8 °C) is rather poor. An alternative is to exploit the exponential behavior of MOSFETs in the subthreshold region [1], [8], [9]. Such sensors can operate from sub-1-V supplies, but at high temperatures, their accuracy is limited by leakage currents [1]. Thermal diffusivity (TD) sensors can scale well with technology and power supply, and can achieve moderate accuracy [2], [10]. However, they typically draw several milliwatts, which is a serious drawback in thermal management applications.

Recently, temperature sensors based on on-chip resistors have been proposed [11]–[20]. Being passive components, resistors can be implemented in any process and operated at any supply voltage. In standard CMOS processes, several types of resistors are available: N-well, metal, diffusion, and poly-silicon resistors. Of these, poly-silicon resistors have a low-voltage dependence, low 1/f noise, and a reasonably linear temperature dependence. They can also be combined with a silicide layer, which further increases their temperature coefficient (TC). Temperature sensors based on the temperature-dependent phase shift of RC Wien-bridge (WB) filters [12]–[14] or the temperature-dependent output current of Wheatstone-bridges (WhB) [15]–[17] have been realized. They can achieve high resolution in an energy-efficient manner by utilizing delta–sigma (ΔΣ) modulator-based readout circuits but occupy considerable area (0.72 mm² in [14] and 0.25 mm² in [16]). In contrast to WB sensors, WhB sensors do not require an external frequency reference [15], [16], and...
can be read out by area-efficient SAR ADCs [17]. However, the reported area, 0.044 mm² in [17], is still too large for on-chip thermal management applications.

This paper presents a compact energy-efficient resistor-based CMOS temperature sensor, which is based on the combination of an RC poly-phase filter (PPF) and a frequency-locked loop (FLL) [18]. Compared to WB filters, PPFs provide higher frequency-to-phase gain and larger voltage swing, allowing the synchronous phase detectors of previous work to be replaced by a much simpler zero-crossing (ZC) detector. This then forms the heart of an area-efficient FLL. A prototype sensor, implemented in 65-nm standard CMOS process, occupies only 7000 μm². It operates at supply voltages from 0.85 V and consumes 68 μW. After a two-point trim, the silicided p-poly sensor achieves an inaccuracy of ±0.12 °C (3σ) from −40 °C to 85 °C and 2.5-mK rms resolution in a 1-ms conversion time, which corresponds to a competitive resolution figure-of-merit (FoM) of 0.43 pJ·K².

This paper is organized as follows. Section II reviews conventional resistor-based temperature sensors, and Section III explains the proposed resistor-based temperature sensor. Section IV describes the implementation details, and Section V shows measurement results. Finally, the conclusion is presented in Section VI.

II. CONVENTIONAL RESISTOR-BASED TEMPERATURE SENSORS

A resistor-based sensor can be implemented by either sensing the temperature-dependent phase shift of RC filters [12]–[14] or the ratio of two resistances with different TCs [15], [16]–[17]. This section describes two representative types of resistor-based sensors: WB sensors and WhB sensors.

A. Wien-Bridge Sensor

WB sensors, which are based on the 2nd-order RC bandpass filters (BPF), have been proposed for temperature sensing because their temperature-to-phase characteristic has a higher TC and better linearity than a simple 1st-order low-pass filter (LPF) [12]–[14]. The temperature dependence of a WB will be mainly determined by its resistors, because on-chip capacitors are comparatively insensitive to temperature. As shown in Fig. 1(a), for a sinusoidal input voltage $V_{IN}$, the output current $I_{WB}$ is given by

$$I_{WB}(j\omega) = \frac{Cj\omega}{1 - R^2C^2\omega^2 + 3RCj\omega}$$

and the phase shift of the WB $\phi_{WB}(\omega)$ is

$$\phi_{WB}(\omega) = \tan^{-1} \frac{1 - R^2C^2\omega^2}{3RC\omega}$$

which is 0 at the filter’s center frequency $f_0 = 1/(2\pi RC)$.

As an example, consider a WB realized from silicided n-poly resistors and metal–insulator–metal (MIM) capacitors in the TSMC 65-nm CMOS process. When driven at a fixed $f_0$, $\phi_{WB}$ will then vary from 8° to −4° over the industrial temperature range (−40 °C–85 °C). On the other hand, when $\phi_{WB}$ is regulated to 0, the center frequency $f_0$ varies from 11.25 to 8 MHz over the same temperature range, as shown in Fig. 1(b).

To accurately determine the filter’s phase shift, synchronous phase detectors are often used [13], [14]. As shown in Fig. 2, such a detector consists of a chopper demodulator followed by an LPF. For a filter driven by a periodic input, typically a square-wave, the dc component of the detector’s output $V_{DC}$ will be proportional to the filter’s $RC$ time constant, which, in turn, is proportional to its phase shift. In this arrangement, the noise bandwidth is defined by the LPF, whose cutoff frequency $F_C$ must be low enough to achieve the necessary resolution and suppress the even-order harmonics generated by the chopper demodulator. Therefore, large filter capacitors are often required, resulting in a large area (0.09 mm² in [13] and 0.72 mm² in [14]).

B. Wheatstone-Bridge Sensor

As shown in Fig. 3(a), a WhB sensor consists of two different types of resistors ($R_1$ and $R_2$), which have similar resistances at room temperature but different TCs [15], [16]. When connected to a virtual ground, e.g., the input of an active integrator, the WhB will output a temperature-dependent current $I_{WhB}$. By combining resistors with opposite TCs ($a_1$ and $a_2$) [16], the TC of the output current ($=a_1-a_2$) can be larger than that of a single resistor, as shown in Fig. 3(a).

An energy-efficient way to read out $I_{WB}$ is by directly applying it to the input of a continuous-time $\Delta \Sigma$ modulator (CT$\Delta \Sigma$M), as shown in Fig. 3(b). As temperature changes,
Fig. 3. (a) Schematic of the WhB and its current characteristics over temperature and (b) its CTΔΣM-based readout scheme.

$I_{WhB}$ is continuously balanced by the current $I_{DAC}$ from a resistive DAC. The resulting digital output of the modulator, $D_{OUT} = I_{WhB}/I_{DAC}$, mainly depends on the TCs of the WhB resistors. The enhanced TC of the sensor and the CTΔΣM readout lead to both high resolution and high energy-efficiency (32 fJ·K² in [16]).

However, this comes at the expense of area because the capacitors of the 1st integrator need to be large enough to filter the quantization noise of the DAC, resulting in a relatively large area of 0.43 mm² in [15] and 0.25 mm² in [16]. Moreover, unlike a WB sensor, a WhB sensor uses, at least, two types of resistors. As a result, its accuracy is more vulnerable to process spread, especially when implemented in a small area. These considerations make WhB-based sensors less attractive for use in dense thermal monitoring applications.

III. PROPOSED RESISTOR-BASED TEMPERATURE SENSOR

A. Proposed Zero-Crossing Detection Scheme

Fig. 4 illustrates the proposed ZC detection scheme, which consists of a ZC detector and a digital phase/frequency detector (PFD). When an RC filter is driven by a fixed frequency $F_{DRV}$, the shape of its output waveform ($V_{RC}$) will depend on the filter’s time-constant. In practice, a differential topology will be used, as shown in Fig. 4(b). When $V_{RC+}$ and $V_{RC−}$ reach the threshold voltage $A/2$, the ZC point of their differential voltage will be sensed by a ZC detector, resulting in the output signal $V_{ZC}$. A digital PFD then compares the rising edges of $F_{DRV}$ and $V_{ZC}$ and provides a digital pulse $F_{RC}$ with a duty cycle $T_0$. A key observation is that $T_0$ is proportional to the phase shift $\phi_{RC}$, which contains the desired temperature information. Compared to a synchronous phase detector, a ZC detector does not need a narrow-band LPF, which often requires large capacitors, resulting in a more compact implementation. Even so, the filter’s absence results in less resolution because the front-end’s wide-band noise is not filtered.

B. Poly Resistors in CMOS Process

In [12]–[14] and [16], poly resistors in a 0.18-μm CMOS process were used as sensing elements because of their high TC and high stability over a wide temperature range. To investigate the impact of process scaling, the characteristics of poly resistors are compared in two different process nodes (TSMC 65-nm and 0.18-μm CMOS), as shown in Table I. In both nodes, the use of a silicide layer increases their TCs (5 × in 65-nm CMOS and 2 × in 0.18-μm CMOS). In 65-nm CMOS, however, the sheet resistance of the silicided poly resistor increases by 2 ×, leading to proportionally smaller resistors. Although the silicided poly resistors in 65-nm CMOS have a more non-linear temperature dependence as in [21], this can be corrected in the sensor’s digital back end [12]. These considerations led to the choice of silicided poly resistors as being the most suitable temperature-sensing resistors available in the target 65-nm CMOS process.

C. PPF-Based Temperature Sensor

To better utilize the properties of the sensing resistors, an RC PPF is proposed as a temperature sensor. Fig. 5(a) shows the schematic of a PPF sensor, which, like a 1st-order RC LPF, consists of a pair of resistors and capacitors. Both ends of the RC PPF are driven by anti-phase clocks ($\pm V_{IN}/2$).
The output voltage $V_{PPF}$ to the differential input voltage $V_{IN}$ is then given by

$$V_{PPF}(j\omega) = \frac{1 - RCj\omega}{1 + RCj\omega}$$

and the phase shift of the PPF $\phi_{PPF}(\omega)$ is

$$\phi_{PPF}(\omega) = 2 \cdot \tan^{-1}(-RC\omega).$$

Fig. 5(b) shows the phase response of three RC filters with normalized characteristic frequencies with $f_0 = 1/(2\pi RC)$. As can be seen, the positive zero in (3) results in a 2nd-order phase response. Therefore, compared to the 1st-order LPF, the frequency-to-phase gain of the PPF is doubled at $f_0$: $d\phi_{PPF}/d\omega = -RC$, which is also $1.5 \times$ larger than that of the WB filter: $d\phi_{WB}/d\omega = -2/(3RC)$. As shown in Fig. 6, when driven at a fixed $f_0$, the PPF’s phase shift is $18^\circ$ over the industrial temperature range, $1.5 \times$ larger than the WB filter’s ($12^\circ$). On the other hand, when the phase shift is adjusted to 0, the frequency shift for both the WB filter and the PPF is the same. Moreover, since the number of PPF elements ($2R$ and $2C$) is less than that of the WB sensor ($4R$ and $3C$), the PPF can be implemented in a more area-efficient way.

Fig. 7 illustrates the operation of the PPF sensor with its output voltage waveform. It is driven by anti-phase clocks of $f_0$ with a voltage swing of $V_A$. During the charging phase $\phi_1$, the capacitor is charged to an intermediate voltage $V_C$, and the ZC point occurs after one quarter of the driving period ($T/4$). During the discharging phase $\phi_2$, the output voltage $V_{PPF}$ is initially boosted to $V_C + V_A$ due to the capacitive coupling and then starts to discharge via $R(T)$. After the discharging phase, a negative boosting also happens at the start of the next phase $\phi_1$. Therefore, the signal swing of the PPF sensor can be much larger compared to other RC-based sensors [22].

**Given a square-wave input with duty cycle $t_{ON}$ and period $T$, the periodic steady-state response $V_{PSS}$ is given by**

$$V_{PSS}(t) = V_A \left\{1 - 2e^{-\frac{t}{RC}} \left( e^{\frac{\pi RC}{4}} - 1 + e^{-\frac{\pi RC}{4}} \right) \right\} (0 < t < t_{ON})$$

$$= 2V_A \cdot e^{-\frac{t}{RC}} \left( \frac{e^{\frac{\pi RC}{4}}}{1 + e^{-\frac{\pi RC}{4}}} \right) (t_{ON} < t < T).$$

**D. Proposed PPF-Based FLL**

Based on the fact that the PPF’s phase shift is $-90^\circ$ at $f_0$, it can be read out by embedding it in an FLL and forcing the phase difference between its ZC output and the quadrature-phase signal of $f_0$ to be 0. Fig. 8 shows the block and timing diagrams of the proposed PPF-based FLL. The output frequency $F_{PPF}$ of a current-controlled oscillator (CCO) is divided by 4 to provide an in-phase feedback signal (P) for the PPF ($R = 35 \, k\Omega$ and $C = 0.5 \, pF$) and a quadrature-phase signal ($Q$) for the PFD. The ZC of the sensor output ($V_{PPF}$) is converted into $V_O$ via the ZC detector, which is implemented by a comparator. As shown in Fig. 8(b), if the phase error $\phi_{DIFF}$ between $V_O$ and $Q$ occurs, a digital tri-state PFD provides up or down signal into a charge pump (CP), whose output current flows into an integration capacitor ($C_{INT}$) of the loop filter and controls its output current $I_{INT}$ by a $g_m$ stage. $I_{INT}$ is then adjusted to drive $\phi_{DIFF}$ to 0. At steady state, $F_{PPF}$ is locked to four times the PPF’s center frequency, where the PPF’s phase shift $\phi_{LOCK}$ is $90^\circ$.

Since the PPF’s phase shift is always less than $180^\circ$, the ZC point also occurs within a half duty-cycle. Therefore, the ZC detector can be duty-cycled around the ZC point to reduce its power consumption. The division ratio of the divider can be...
the FLL is shown in Fig. 9(a), where $K_P$ is the frequency-to-
phase gain of the sensor, $K_I$ is the PFD/CP gain, and $K_{CCO}$ is
the CCO tuning gain. The front-end noise from the PPF sensor
and the ZC detector is defined as the phase noise $\phi_{n,IN}$, which
results from the output-referred voltage noise ($V_{n,R}$) of the
sensing resistor and the input-referred voltage noise ($V_{n,ZC}$) of
the ZC detector. The total voltage noise ($V_{n,IN}$) of the front
end is given by

$$V_{n,IN}^2 = V_{n,R}^2 + V_{n,ZC}^2. \tag{6}$$

Then, the front-end phase noise can be expressed in terms of
this voltage noise and derived from the timing jitter $t_d$ at the
sensor output and the sensor’s driving frequency $f_0$ [23]. The
jitter is determined by the voltage noise $V_{n,IN}$ and the slope
of the sensor output voltage at the ZC point (i.e., $t = T/4$)
and can be calculated by using the derivative $dV/dt$ from (5).
Therefore, the front-end phase noise can be calculated as

$$\phi_{n,IN}^2 = (2\pi f_0 t_d)^2 = \left(2\pi f_0 \frac{dV}{V_{n,IN}}\right)^2 = \frac{V_{n,IN}^2}{A^2} \tag{7}$$

where $A$ is the peak-to-peak voltage swing of $f_0$.

At steady state, the output of the PFD will be a short pulse
with a duration $t_{PFD}$ that is much smaller than the driving
period $t_{DRV}$ [24]. The current noise of the CP ($I_{n,CP}$) can
then be modeled as phase noise as shown in the following:

$$\phi_{n,CP}^2 = \frac{I_{n,CP}^2}{I_{CP}^2} \frac{t_{PFD}}{t_{DRV}}. \tag{8}$$

where $I_{CP}$ is the output current of the CP.

For simplicity, the phase noise of the front end and the CP
is combined into $\phi_n^2 = \phi_{n,IN}^2 + \phi_{n,CP}^2$ at the sensor output.
The noise transfer function (NTF) from $\phi_n$ to $F_{OUT}$ can be
calculated as

$$H_{IN}(s) = \frac{F_{OUT}(s)}{\phi_n(s)} = \frac{1}{2\pi} \frac{K_{I} \frac{gm}{s_{INT}} 2\pi K_{CCO}}{1 + \frac{K_{P}}{N} \frac{gm}{s_{INT}} 2\pi K_{CCO}} \tag{9}$$

where $G(s)$ is the open-loop transfer function of the FLL.
(Thus, $G(s) \gg 1$ near dc.) While $\phi_n$ is low-pass filtered
by its NTF, it can be seen that $gm$ current noise $I_{n,gm}$ and
the CCO phase noise $\phi_{n,CCO}$ are high-pass filtered by each
NTF ($H_{gm}$ and $H_{CCO}$). From (6)–(9), the power spectral
density (PSD) of the FLL’s output frequency noise $S_{FOUT}(f)$
can be expressed as

$$S_{FOUT}(f) = S_n(f) \cdot |H_{IN}(f)|^2 + S_{gm}(f) \cdot |H_{gm}(f)|^2 + S_{CCO}(f) \cdot |H_{CCO}(f)|^2 \tag{10}$$

where $S_n(f)$, $S_{gm}(f)$, and $S_{CCO}(f)$ are the PSDs of the phase
noise at the sensor output, the $gm$ current noise, and the CCO
phase noise, respectively. Since an off-chip counter digitizes
the FLL’s output frequency $F_{OUT}$ by counting the number
of the edges of $F_{OUT}$, it works as a sinc filter with a time
length $t_{conv}$. This means filtering out $F_{OUT}$ with a noise
bandwidth of $(2t_{conv})^{-1}$ [13]. As a result, the RMS frequency
noise can be easily calculated by integrating $S_{FOUT}(f)$ up to
the bandwidth.
To estimate the achievable temperature resolution of this sensor, a noiseless readout circuit is assumed with the noise bandwidth smaller than the loop bandwidth. Then, the temperature resolution is limited by the sensing resistor’s thermal noise. Given that the output-referred voltage noise of the sensor is $V_{n,R,\text{out}}^2 = 4kT$, its PSD is folded due to the sampling effect of the PFD [24] as follows:

$$S_{n,R}(f) = 4 kT R_{A}^2. \quad (11)$$

Combining this with (10) and (11), the RMS frequency noise is given by

$$\Delta F_{\text{OUT}} = \sqrt{S_{n,R}(f) \cdot |H_{\text{IN}}(f)|^2} \cdot \frac{1}{2\tau_{\text{conv}}},$$

$$= \frac{N}{\pi AC} \sqrt{\frac{kT}{\tau_{\text{conv}} R}}. \quad (12)$$

The temperature resolution is then calculated by dividing $\Delta F_{\text{OUT}}$ into its temperature sensitivity. Given that the TC of the resistor is $\alpha$ and the resistance at room temperature is $R_0$, the resolution $\Delta T$ at room temperature is calculated as follows:

$$\Delta T = \Delta F_{\text{OUT}} \cdot \frac{dT}{dF_{\text{OUT}}} = \frac{N}{\pi AC} \sqrt{\frac{kT}{\tau_{\text{conv}} R}} \frac{2\pi R_0 C}{Na}$$

$$= \frac{2}{\alpha A} \sqrt{\frac{kT R_0}{\tau_{\text{conv}}}}. \quad (13)$$

In the actual design, the PPF sensor is implemented with $R_0 = 35 \, \text{k}\Omega$ and $A = 1 \, \text{V}$. As shown in Fig. 9(b), a PPF sensor based on silicided p-poly resistors has a fundamental temperature resolution of 288 $\mu\text{K}_{\text{rms}}$ at $\tau_{\text{conv}} = 1 \, \text{ms}$. In practice, the temperature resolution is degraded by the noise added by the following blocks: the ZC detector, the CP, the $g_m$ stage, and the CCO. Since their NTFs are formed by the FLL, the noise of $g_m$ stage and the CCO and the front-end noise are high-pass and low-pass filtered, respectively. Now, consider an estimated loop bandwidth of 20 kHz, which is equivalent to a conversion time of 25 $\mu$s. Then, at $\tau_{\text{conv}} > 25 \, \mu$s, the resolution is limited by 1/f noise of the ZC detector and the CP. In the opposite case, the thermal noise of CCO and 1/f noise of $g_m$ stage are dominant sources of the total noise. Consequently, the resolution is estimated to be 1.95 m$\text{K}_{\text{rms}}$ at $\tau_{\text{conv}} = 1 \, \text{ms}$.

### IV. IMPLEMENTATION

Fig. 10 shows the full block diagram of the proposed PPF-based FLL readout. The loop filter of the readout circuits consists of a push–pull CP (CP_{INT}), a push-type CP (CP_{SU}), an integration capacitor $C_{\text{INT}}$, and a $g_m$. In Sections IV-A–IV-C, each block will be described in detail.

#### A. ZC Detector

Fig. 11 shows the schematic of the ZC detector. It is implemented as a two-stage inverter-based comparator to facilitate scaling in advanced processes [25]. Two inverters serve as a preamplifier, which then drives a cross-coupled latch. As shown in Fig. 11(b), the output voltage $V_{\text{PPF}}$ of the PPF sensor is only sampled on the rising edge of quadrature-phase signal $Q$ in Fig. 8(b). Then, to reduce the power consumption, the ZC detector can be disabled and reset by turning off the first stage. Therefore, its averaged current can be reduced from 20.5 to 10.9 $\mu\text{A}$. Moreover, the periodic switching of both the enable and reset switches can reduce the 1/f noise of the input transistors [26]. From simulations, the input-referred noise is reduced from 38.26 to 8.76 $\mu\text{V}_{\text{rms}}$. 

![Fig. 11. (a) Schematic of the ZC detector and (b) its operating principle.](image-url)
For the silicided p-poly sensor with a 1-ms conversion time, it improves temperature resolution from 6.48 to 1.95 mK$_{\text{rms}}$, thus leading to the high resolution. From Monte Carlo simulations, the variation of the offset voltage is $\pm 12.5$ mV, which translates into a temperature inaccuracy of $\sim 0.06 \, ^\circ\text{C} (3\sigma)$ after digital calibration, as will be described in Section V-B.

Since the PPF’s output peak voltage is about $1.87 \times$ the supply voltage, it can exceed the maximum gate voltage allowable at the detector’s input transistors. So, the supply voltage of this paper is limited to 1.05 V in the chosen process.

To accommodate higher supplies, the input transistors should be realized with thick-oxide devices.

### B. Loop Filter

The schematic of the loop filter combined with the CCO is shown in Fig. 10. The loop filter is composed of a startup path and an integral path. To start the current-starved oscillator, a pull-up circuit is implemented in a push-type CP (CP SU), which avoids mismatch by using only PMOS current sources [27]. Moreover, the startup path ($I_{SU}$) reduces the locking time of the loop from power-on–reset condition, which is important for dense thermal monitoring. Consequently, the locking time (cycle) is decreased by $2 \times$ from $\sim 6.8$ (70 cycles) to $\sim 3.4$ $\mu$s (35 cycles). As shown in Fig. 12, the locking time (cycle) varies between $\sim 3$ (20 cycles at 75 $^\circ\text{C}$ of SS corner) and $\sim 4.5$ $\mu$s (90 cycles at -40 $^\circ\text{C}$ of FF corner) across the process, voltage and temperature (PVT) variations.

The CP of the integral path, CP INT, controls the bias voltage $V_B$ across $C_{\text{INT}}$ to generate $I_{SU}$ and $I_{\text{INT}}$ (5 and 10 $\mu$A at steady state) via PMOS transistors (M1–M3). Then, both currents are summed at the CCO’s supply node ($V_{\text{CCO}}$). Depending on the PFD state, i.e., up, reset, and down, $I_{SU}$ is weighted by 2, 1, and 0, respectively. This is performed by two switches that are controlled by the PFD outputs ($UP$ and $DN$). Since $I_{SU}$ is generated from CP INT, it works as an added $g_m$ (120 $\mu$S) and increases the loop bandwidth to about 20 kHz, reducing the CCO phase noise effectively. From Monte Carlo simulations, matching error between two current sources of CP INT is $\pm 3.5\%$, which translates into a temperature inaccuracy of $\sim 0.04 \, ^\circ\text{C} (3\sigma)$ after digital calibration, as will be described in Section V-B.

### C. CCO

As shown in Fig. 13, the CCO is designed as a nine-stage current-starved ring oscillator, whose tuning gain

$K_{\text{CCO}}$ is 1 MHz/$\mu$A. It achieves the target output frequency range from 38 to 52 MHz for both silicided n-poly and p-poly sensors. Its delay cell consists of two inverters cross-coupled with each other in a feed-forward manner using transmission gates, which attenuates the common-mode signals by ensuring pseudo-differential operation [28]. As shown in Fig. 10, following the CCO output, the output buffer achieves rail-to-rail operation and 50% duty cycle via a level-shifter and an inverter-based latch, respectively.

### V. Measurement Results

The sensor is fabricated in 65-nm standard CMOS technology, and the chip micrograph is shown in Fig. 14(a). For flexibility, a counter, a digital back end, and current bias circuits were implemented off-chip. Each sample contains
two different sensors: one with silicided p-poly (s-p-poly) resistors and the other with silicided n-poly (s-n-poly) resistors, shown in [18]. We use an off-chip bias current and the current is copied to each sensor. The current is set at room temperature, and the sensor’s temperature inaccuracies are measured by using the fixed bias current. When an on-chip bias current is used, changes in bias current might affect the mismatch between the CP’s up and down current, which causes temperature inaccuracy. Assuming the use of a simple bootstrapped current source [30] with a 4% spread, this results in a temperature inaccuracy of 10 mK after a two-point trim. Therefore, its impact is negligible. For both sensors, 16 samples in ceramic dual in-line packages are characterized from $-40$ °C to 85 °C in a temperature-controlled oven, in which the actual temperature of the sensor is established by a platinum Pt-100 resistor sensor. Each sensor occupies only the active area of 7000 $\mu$m$^2$, 40% of which is occupied by the PPF sensor, as shown in Fig. 14(b). It draws 68 $\mu$A from a 1-V supply, and its power breakdown is also described in Fig. 14(c). The CCO with the loop filter and the PPF driver dissipate about 71% of the power consumption. At room temperature, a supply sensitivity of 0.5 °C/V is measured for supply voltages from 0.85 to 1.05 V.

A. Noise and Temperature Resolution

Fig. 15 shows the measured sensors’ output frequencies: 48–38 MHz for s-n-poly sensors (0.19%/°C) and 52–40 MHz for s-p-poly sensors (0.22%/°C), respectively. Since the TC of s-p-poly sensor is about 15% higher than that of s-n-poly sensor, it can be seen that the resolution of s-p-poly sensor is better than that of s-n-poly sensor. Fig. 16 shows the measured phase noise of FLL’s output (s-n-poly sensor) with the estimated noise contributions of the front end, CP, $g_m$, and CCO. With the loop bandwidth of 20 kHz, it can be seen that the CCO and

$g_m$ noise are high-pass filtered, and the front end and the CP noise are low-pass filtered. The measured phase noise is $-124$ dBc/Hz at 100 kHz offset, and the RMS jitter integrated from 1 Hz to 100 kHz is 12 ps. As shown in Fig. 17, the accumulated jitter for both sensors is plotted versus the
number of cycles, and it can be measured in a fixed time window corresponding to a conversion time. The accumulated jitter increases up to $10^4$ cycles with $\sqrt{N}$ behavior due to thermal noise, while showing $N$ behavior by the $1/f$ noise after the cycles. The temperature resolution is determined by the accumulated jitter and the TC of the output period within the operating temperature range, as shown in Fig. 17(b). For a 1-ms conversion time, the accumulated jitters of 5.2 ns (rms) for s-n-poly sensor and 5.23 ns (rms) for s-p-poly sensor are measured, which correspond to the temperature resolutions of 2.8 and 2.5 mK, respectively. Therefore, the sensor can track millisecond thermal transient with a few millikelvin temperature resolutions.

There are several ways to digitize an oscillator’s output [1], [8], [9], [13], [20]. Considering an on-chip counter driven by a lower reference frequency, the sensor’s output frequency can be digitized by using one or more clock cycles to determine the gating time of the counter. For instance, given a 1-ms gating time of the counter, the quantization noise can be translated to a temperature noise of about 3 mK (rms), in which case, the non-linearity function of the sensor may be limited by quantization noise. However, the quantization noise can also be reduced by using the CCO’s multi-phase information as in [13].

B. Systematic Non-Linearity Correction and Calibration

The PPF sensor’s output frequency is directly affected by the sensing resistor and the MIM capacitor. Since the MIM capacitor’s TC is very low (~15 ppm/°C), the resistor’s TC mainly determines the sensor’s temperature dependence. As described in Section III-B, however, the resistors have a non-linear temperature dependence, which leads to increased inaccuracy and needs to be removed. After a 1st-order linear fit of the sensor’s output frequency, only the systematic non-linearity remains, as shown in Fig. 18. Then, it is fit with a fixed polynomial (fifth-order) function [14]. Thus, the non-linearity function is corrected from the measured output in the digital back end, and the linearly calibrated output can be finally obtained.

As shown in Fig. 19, after one- and two-point trim with the removal of the systematic non-linearity, the s-n-poly sensor achieves a $3\sigma$ inaccuracy of ±3.65 °C and ±0.35 °C, while the s-p-poly sensor achieves a $3\sigma$ inaccuracy of ±3 °C and ±0.31 °C. It should be noted that the output frequency of the FLL is proportional to $1/RC$ and thus the systematic non-linearity of the resistor also appears inversely at the output. This makes the non-linearity of the output much larger than that of the resistor and interferes with a precise 1st-order linear fit. As a result, the sensor’s spread with larger non-linearity further increases the inaccuracy. However, since the output period of the FLL is directly proportional to $RC$, the remaining non-linearity after a 1st-order period-fit is less than that after a 1st-order frequency-fit for both sensors, as shown in Fig. 18. As shown in Fig. 20, the resulting inaccuracy after one- and two-point trim following the proposed period-fit has decreased to ±2.47 °C (3\sigma) and ±0.12 °C (3\sigma) for s-p-poly sensor. The spread sources of s-p-poly sensor’s inaccuracy consist of 50% for the offset voltage of the ZC.
TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH OTHER STATE-OF-THE-ART WORKS

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Readout Type</td>
<td>FLL</td>
<td>FLL</td>
<td>ΔΣ</td>
<td>OSC</td>
<td>OSC</td>
<td>ΔΣ</td>
<td>ΔΣ</td>
</tr>
<tr>
<td>Technology</td>
<td>65nm</td>
<td>180nm</td>
<td>180nm</td>
<td>16nm</td>
<td>180nm</td>
<td>14nm</td>
<td>40nm</td>
</tr>
<tr>
<td>Area (μm²)</td>
<td><strong>7000</strong></td>
<td>90000</td>
<td>250000</td>
<td>15000</td>
<td>8865</td>
<td>7800</td>
<td>1650</td>
</tr>
<tr>
<td>Power (μW)</td>
<td>68</td>
<td>31</td>
<td>94</td>
<td>70</td>
<td>0.075</td>
<td>1100</td>
<td>2500</td>
</tr>
<tr>
<td>Supply voltage (V)</td>
<td>0.85–1.05</td>
<td>3.3</td>
<td>1.6–2</td>
<td>0.7</td>
<td>0.8–1.8</td>
<td>1.35</td>
<td>0.9–1.2</td>
</tr>
<tr>
<td>Supply sensitivity (°C/V)</td>
<td>0.5</td>
<td>0.4</td>
<td>0.02</td>
<td>-</td>
<td>0.13</td>
<td>-</td>
<td>2.8</td>
</tr>
<tr>
<td>Temperature range (°C)</td>
<td>-40 to 85</td>
<td>-40 to 85</td>
<td>-55 to 125</td>
<td>-10 to 90</td>
<td>-20 to 100</td>
<td>0 to 100</td>
<td>-40 to 125</td>
</tr>
<tr>
<td>Inaccuracy (°C)</td>
<td>±0.12**</td>
<td>±0.12**</td>
<td>±0.12**</td>
<td>±1**</td>
<td>±0.22/0.19**</td>
<td>±0.7**</td>
<td>±0.75**</td>
</tr>
<tr>
<td>(°C)</td>
<td>(3σ)</td>
<td>(3σ)</td>
<td>(3σ)</td>
<td>(3σ)</td>
<td>(3σ)</td>
<td>(3σ)</td>
<td></td>
</tr>
<tr>
<td>Conversion time (ms)</td>
<td>1</td>
<td>32</td>
<td>5</td>
<td>1.6</td>
<td>8</td>
<td>0.02</td>
<td>1</td>
</tr>
<tr>
<td>Energy/Conversion (nJ)</td>
<td>68</td>
<td>992</td>
<td>470</td>
<td>112</td>
<td>0.6</td>
<td>22</td>
<td>2500</td>
</tr>
<tr>
<td>Resolution (°C)</td>
<td>0.0025</td>
<td>0.0028</td>
<td>0.00026</td>
<td>1</td>
<td>0.073</td>
<td>0.5</td>
<td>0.36</td>
</tr>
<tr>
<td>Resolution FoM (pJ·K⁻²)</td>
<td>0.43</td>
<td>8</td>
<td>0.032</td>
<td>112000</td>
<td>3.2</td>
<td>5500</td>
<td>324000</td>
</tr>
</tbody>
</table>

1 Estimated area including on-chip bias and 16-bit counter in the chosen process
2 1-point trimming, ** 2-point trimming, *** 3-point trimming

![Resolution FoM versus area for CMOS smart temperature sensors.](image)

The performance of the sensor based on the s-p-poly resistors is summarized in Table II and compared to other compact energy-efficient CMOS temperature sensors. After a two-point trim, the sensor achieves an inaccuracy of ±0.12 °C (3σ), which is comparable to that of state-of-the-art sensors. It achieves a competitive energy-efficiency of 0.43 pJ·K⁻², only occupying the area of 7000 μm². Even if the estimated area of the on-chip bias and counter in the chosen process is considered, the total area would be 7700 μm². As shown in Fig. 21, this work is 13× smaller than a WB-based FLL sensor [13] and significantly smaller than a WhB-based sensor with CTDMSM [16]. Due to the supply-voltage scaling and improved jitter performance, the resolution FoM of this work is also highly improved by 18× compared to [13]. The size of this work is very close to that of a compact MOS-based sensor [9], while achieving 7× improvement on energy-efficiency. Compared to the state-of-the-art TD- and BJT-based sensors [2], [3], this sensor consumes significantly less energy.

VI. CONCLUSION

A resistor-based CMOS temperature sensor for on-chip thermal monitoring has been implemented in a standard 65-nm CMOS technology. It is based on a PPF implemented with silicided poly resistors and stable MIM capacitors, which provides small area, high TC, and large-signal swing. The PPF’s temperature-dependent phase shift is effectively measured with a ZC detector, which allows implementing an area- and energy-efficient FLL. The prototype sensor occupies only 7000 μm², the smallest among all the resistor-based temperature sensors, and also operates at supply voltages from 0.85 V. The sensor has been characterized with two different resistors (s-p-poly/s-n-poly). The sensor based on the s-p-poly resistors achieves a resolution of 2.5 mK rms in a 1-ms conversion time, corresponding to a competitive resolution FoM of 0.43 pJ·K⁻². After a two-point calibration, the sensor achieves an inaccuracy of ±0.12 °C (3σ) from −40 °C to 85 °C, which is also comparable to the state-of-the-arts. These results demonstrate that the proposed resistor-based sensor is suitable for realizing a reliable temperature sensor for dense thermal monitoring in nanometer CMOS.

REFERENCES


Woojun Choi (S’15) received the B.S. degree in electrical and electronic engineering from Yonsei University, Seoul, South Korea, in 2015, where he is currently pursuing the Ph.D. degree in electrical and electronic engineering. He is being supported by the National Research Foundation of Korea (NRF-2016-Global Ph.D. Fellowship Program). His current research interests include high-speed interface circuits, precision analog circuits, and CMOS temperature sensors.

Yongtae Lee (S’16) received the B.S. degree in electrical and electronic engineering from Yonsei University, Seoul, South Korea, in 2016, where he is currently pursuing the Ph.D. degree in electrical and electronic engineering. His current research interests include low-power, high-accuracy temperature sensors.

Seonhong Kim received the B.S. degree in electrical engineering from Inha University, Incheon, South Korea, in 2011. He joined the DRAM Design Division, SK Hynix, Incheon, in 2012, where he has worked on analog circuit design and temperature sensor in the Circuit Design Team. He was involved in the circuit design of low-power mobile DRAM.
Sanghoon Lee received the B.S. degree in electrical engineering from Sungkyunkwan University, Suwon, South Korea, in 2011.

He joined SK Hynix, Icheon, South Korea, in 2012, where he has been working on generator and temperature sensor of DDR4 and LPDDR4 in the Circuit Design Team.

Jieun Jang joined SK Hynix, Icheon, South Korea, in 1997, where she has been in charge of the DDR4 Circuit Design Team since 2017. She is engaged in the development of high-speed, low-power DDR4.

Junhyun Chun received the B.S. degree in electrical engineering from Kyungpook National University, Daegu, South Korea, in 1991.

He joined SK Hynix, Icheon, South Korea, in 1992, where he is currently the Vice President and the Head of the Circuit Design Group.


From 1989 to 1999, he was a Research Scientist with the Philips Research Laboratories, Eindhoven, where he worked on interactive displays and digital recording systems. In 1999, he joined the Delft University of Technology, where he is currently an Antoni van Leeuwenhoek Professor and the Head of the Microelectronics Department. He has authored 15 books and over 250 technical papers. His current research interests include the design of mixed-signal circuits, sensor interfaces, and smart sensors.

Dr. Makinwa is a member of the Royal Netherlands Academy of Arts and Sciences and the Editorial Board of the PROCEEDINGS OF THE IEEE.

He received the 2005 Simon Stevin Gezel Award from the Dutch Technology Foundation, for his doctoral research. He was recognized as a top-10 contributor of the International Solid-State Circuits Conference (ISSCC). He was a co-recipient of 15 best paper awards from the Journal of Solid-State Circuits (JSSC), ISSCC, Very Large Scale Integration (VLSI), European Solid-State Circuits Conference (ESSCIRC), and Transducers. He is the Analog Subcommittee Chair of ISSCC. He is also on the program committees of the VLSI Symposium, ESSCIRC, and the Advances in Analog Circuit Design (AADC) Workshop. He has served as a Guest Editor of JSSC, and a Distinguished Lecturer and an Elected AdCom Member of the IEEE Solid-State Circuits Society.

Youngcheol Chae (M’09) received the B.S., M.S., and Ph.D. degrees in electrical and electronic engineering from Yonsei University, Seoul, South Korea, in 2003, 2005, and 2009, respectively.

From 2009 to 2011, he was a Post-Doctoral Researcher with the Electronic Instrumentation Laboratory, Delft University of Technology, Delft, The Netherlands. Since 2012, he has been a Faculty Member with Yonsei University and is currently an Associate Professor. He focused on low-power data converters and high-performance sensor interfaces. This results in more than 80 technical papers and 30 patents.

Dr. Chae is a member of the Technical Program Committees of the International Solid-State Circuits Conference (ISSCC) and the Asian Solid-State Circuits Conference (A-SSCC). He received the Best Young Professor Award in engineering from Yonsei University in 2018, the Haedong Young Engineer Award from IEE Korea in 2017, the Outstanding Research Award of Yonsei University in 2017, the Outstanding Teaching Award of Yonsei University in 2013 and 2014, a Research Grant from the Samsung Research Funding Center in 2017, and the VENI Grant from the Dutch Technology Foundation STW in 2011. He is a Distinguished Lecturer (DL) of the IEEE Solid-State Circuits Society (SSCS).