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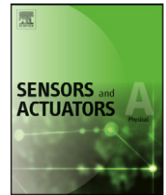

An SOI thermal-diffusivity-based temperature sensor with ±0.6 °C (3σ) untrimmed inaccuracy from −70 °C to 225 °C

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ABSTRACT

This work presents the first thermal-diffusivity-based temperature sensor realized in SOI technology; it has an untrimmed inaccuracy of ±0.6 °C (3σ) from −70 °C up to 225 °C and uses up to 7× less power than prior art. The sensor uses the phase shift of an Electrothermal Filter (ETF) as a proxy for the thermal diffusivity of silicon, D, which has a well-defined $1/T^{1.8}$ temperature dependence. The ETF's output is then digitized by a phase-domain sigma-delta modulator. Measured data from several process lots show that that the sensor's inaccuracy is mainly limited by lithographic spread, and not by wafer-to-wafer or batch-to-batch variations.

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1. Introduction

Because of their small size, low cost, ease of use and digital output, integrated temperature sensors are widely used. Such sensors are typically based on the temperature dependence of bipolar transistors (BJTs). However, because BJTs are intrinsically sensitive to process spread, their untrimmed inaccuracy is limited to a few degrees Celsius. This can be greatly improved by trimming individual devices, but this increases cost. Furthermore, BJTs suffer from exponentially increasing leakage currents at high temperatures, with recent sensors achieving inaccuracies of ±1.0 °C up to 175 °C [2] and ±3.0 °C at 200 °C [3]. The development of such high temperature sensors is driven by the needs of many industrial and automotive applications. However, their inaccuracy is currently much worse than the ±0.1 °C (3σ) inaccuracy that can be achieved at temperatures below 125 °C [1].

An alternative way of measuring temperature is via the thermal diffusivity of silicon, D, which has a $1/T^{1.8}$ temperature dependence. D can be determined by measuring the characteristics of an Electrothermal Filter (ETF), which consists of a heater and a relative temperature sensor realized in the substrate of a silicon chip (Fig. 1). In this structure, power dissipated in the heater generates heat pulses that diffuse through the silicon, creating temperature fluctuations at the sensor. The time it takes for these pulses to diffuse is a function of absolute temperature, or, in other words, the ETF adds a temperature-dependent phase shift, ϕ_{ETF}, to a signal at a single frequency. Because the desired temperature information is now in the time domain, ETFs are unaffected by leakage currents [6]. Additionally, ETFs typically do not require trimming because, for IC-grade silicon, D is well-defined and the distance between the heater and the thermopile, r, is accurately determined by lithography. It has been shown [4,7] that ETFs with equal r achieve untrimmed inaccuracies of ±0.7 °C(3σ) and ±0.2 °C(3σ) in 0.7 μm and 0.18 μm CMOS, respectively, indicating that the dominant source of error is lithographic spread. Moreover, theory [10] and earlier work [5] indicate that D is only weakly sensitive to doping fluctuations at the doping levels typically used in IC technology, which suggests that variations between wafers and process lots should be small.

The characteristics of ETFs in bulk CMOS have been well-documented in prior art [4–7]. Their signal-to-noise ratio (SNR) is rather poor, because a lot of heat is lost to the substrate. This work presents the first ETF in an SOI process, in which the presence of a buried SiO_2 layer significantly reduces this heat loss [20]. Although this is expected to improve the ETF's SNR, the effect on its well-defined characteristics was, up until now, unknown. Based on measurement results from 3 process lots, this work reports on the characteristics of SOI ETF and their device-to-device spread. The measurements show that the effect of changes in doping concentration, wafer-to-wafer and batch-to-batch spread is limited.

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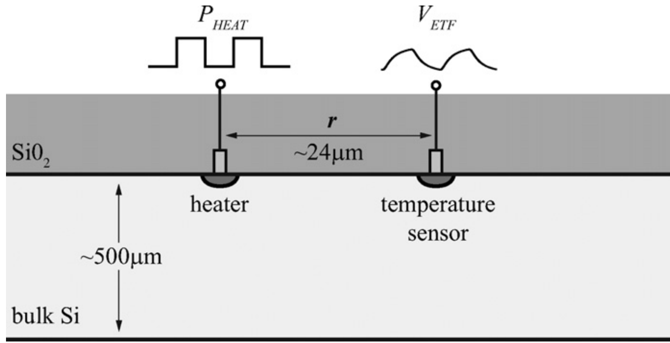

Fig. 1. Schematic side view of a basic Electrothermal Filter (ETF).

The use of an SOI process also enables the implementation of a readout circuit that can operate at very high temperatures, because all devices can be fully isolated, which greatly reduces the effect of leakage current on circuit performance. It has been shown that such circuitry can operate up to 250 °C [8]. In this work, ϕ_{ETF} is digitized by a precision ΣΔ ADC which has been designed to operate up to 250 °C. Measurement results from −70 °C to 225 °C will be presented; this range is mainly limited by test setup considerations.

The next section describes the ETF and its operating principles in greater detail. After discussing its design, analytical and FEM models are used to predict the effect of the buried SiO_2 layer. Section 3 then discusses the readout circuit used to digitize the ETF's output signal and its high-temperature operation, and Section 4 presents the measurement results. The paper ends with conclusions.

2. The Electrothermal Filter

2.1. Basic ETF modeling

As discussed in Section 1, a basic ETF consists of a heater and a temperature sensor, spaced at a distance r in the substrate of a silicon chip (Fig. 1). AC power dissipated in the heater (P_{heat}) creates temperature fluctuations at the sensor, which are low-pass filtered by the substrate's thermal inertia. For typical values of r (∼24 µm), the substrate can be assumed to be infinitely thick, and the SiO_2 layer on top of the silicon is considered to be an ideal insulator. The filtering characteristics of the point-heater, point-sensor ETF in Fig. 1, driven at an angular frequency ω, are expressed by the sensor's *thermal impedance* to the heater, which relates $T(\omega,r)$, the temperature increase at the sensor, to $P_{heat}(\omega)$ [11]:

$$Z_{th}(\omega, r) = \frac{T(\omega, r)}{P_{heat}(\omega)} = \frac{1}{2\pi kr} \exp\left(-r\sqrt{\frac{\omega}{2D}}\right) \exp\left(-jr\sqrt{\frac{\omega}{2D}}\right), \quad (1)$$

in which k is the thermal conductivity and D is the aforementioned thermal diffusivity, which is given by

$$D = \frac{k}{\rho C_p} \quad (2)$$

i.e. the thermal conductivity divided by the heat capacity. For bulk silicon, D is equal to 0.8 cm^2/s at 27 °C and, over the military temperature range, its temperature dependence can be approximated by a $1/T^{1.8}$ power law [4]. When the heater is driven at a frequency f_{drive}, the temperature sensor output has a phase shift, ϕ_{ETF}, which, from Eq. (1), is given by:

$$\phi_{ETF} = -r\sqrt{\frac{\pi f_{drive}}{D}} \quad (3)$$

At constant f_{drive}, ϕ_{ETF} has a near-linear $T^{0.9}$ temperature dependence, which means that ETFs can be used as temperature sensors.

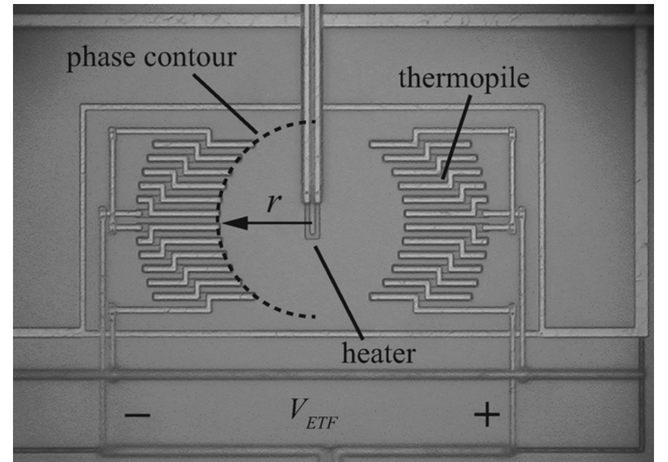

Fig. 2. Top view of an ETF. The thermocouple junctions are positioned on a phase contour to maximize V_{ETF}.

A typical CMOS implementation is more complex than a basic point ETF; Fig. 2 shows the top view of the ETF used in this work. The heater is an n^+-diffusion resistor and the temperature sensor is a thermopile consisting of a series of 48 p+-diffusion/aluminum junctions. At both the hot (nearest to the heater) and cold junctions, a Seebeck voltage develops across the metal-diffusion interface; the location of each thermocouple is, therefore, precisely defined by the contact mask. Fig. 2 structure can be modeled by dividing the heater into a number of point heat sources (P) and calculating the thermal impedance of each thermocouple (N) to these heat sources. Superposition then yields $Z_{th,ETF}$:

$$Z_{th,ETF} = \frac{1}{N}\sum_{n=1}^{N}\sum_{p=1}^{P} Z_{th,hot}(r_{n,p}) - \frac{1}{N}\sum_{n=1}^{N}\sum_{p=1}^{P} Z_{th,cold}(r_{n,p}) \quad (4)$$

To optimize the ETF's transfer function, the heater is designed to mimic a point source and the thermopiles are aligned so that their both their hot and cold junctions each are on equal phase contours [12]. The phase shift of this structure then approximates that of the point-heater, point-sensor ETF, and the lower curve in Fig. 3 shows the simulated $\phi_{ETF}(T)$ for r = 24 µm and f_{drive} = 85 kHz in bulk CMOS. This characteristic and the ETF's $T^{0.9}$ temperature dependence have been confirmed by measurements in earlier work [4].

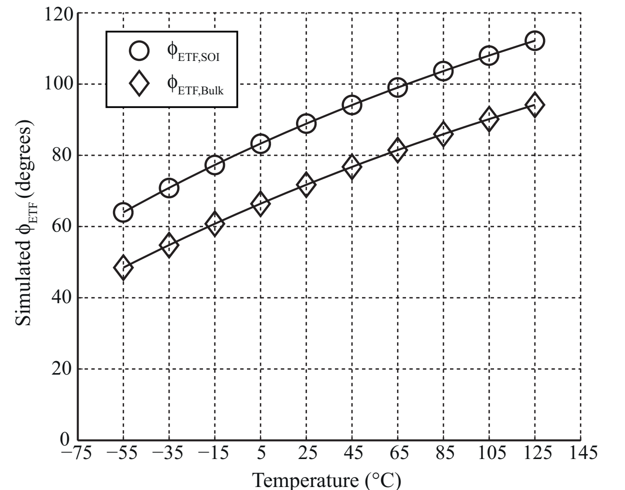

Fig. 3. Simulated ϕ_{ETF} vs. temperature characteristics of ETFs in bulk CMOS and SOI technology.

2.2. Modeling the effect of lithographic spread and doping variations

Variations in ϕ_{ETF} other than those due to changes in T are undesirable, and will lead to temperature-sensing errors. This can be seen by looking at the partial derivatives of Eq. (3):

$$\frac{\partial\phi_{ETF}}{\phi_{ETF}} = \frac{\partial r}{r} = -0.5\frac{\partial D}{D} = 0.9\frac{\partial T}{T} \tag{5}$$

In a typical ETF, the dominant source of temperature error is the spread in r. This, in turn, is a function of the lithographic spread of the process used. Although $\delta r/r$ can be minimized by making r sufficiently large, this results in small signal amplitudes (as per Eq. (1)), so a tradeoff between inaccuracy and resolution exists. Implementations with $r = 24\ \mu$m in 0.7 μm and 0.18 μm CMOS have shown 3σ temperature-sensing errors of ±0.6 °C and ±0.2 °C respectively (see [4,7]); if these errors are solely attributed to lithographic spread, they correspond to values for $\delta r/r$ of 0.14% and 0.045% respectively, or *a* ∼5% (3σ) spread on the minimum feature size of the technology. This work used a 0.5 μm SOI process, and to allow comparison to ETFs in bulk CMOS with the same geometry, r is again set to 24 μm.

For typical doping levels used in IC technology, D is only weakly sensitive to variations in doping. To understand this, a more detailed look at the doping sensitivity of each parameter in Eq. (2) is required. Both ρ and C_p are nearly doping-insensitive: silicon has 5×10^{22} atoms/cm^3, so changes due to e.g. 1×10^{17} dopants/cm^3 are at the ppm-level. The thermal conductivity, however, is somewhat more sensitive. In non-metallic crystals, k is the macroscopic result of phonon transport, and phonon scattering processes prevent k from being arbitrarily large. An expression for k is given by [9]:

$$k = \frac{1}{3}C_p v\lambda \tag{6}$$

in which v is the mean phonon velocity and λ the mean free path associated with phonon scattering. Although phonon–phonon interactions dominate at temperatures beyond ∼100 K [9], small reductions in k due to phonon-impurity scattering have been measured. An excellent discussion is found in [10], in which a model for the doping sensitivity of k_{Si} is provided. This model has been used to calculate the effective value of λ for different doping concentrations so that, through Eq. (2), the doping sensitivity of D can be modeled.

Both the effects of spread in lithography and doping fluctuations can be simulated for an ETF, using the model described in Eq. (4). Lithographic spread was simulated by adding random errors to each contact location, with $\sigma = 10\%$ of the minimum feature size. Fig. 4 shows the (positive) 3σ limits for phase and temperature errors based on 100 trials in both 0.18 μm and 0.7 μm technology. Spread due to doping variations was simulated in a similar way, by setting $\sigma = 10\%$ of the nominal doping level and calculating the effective D_{si} based on the model in [10]. It can be seen that for doping levels below 10^{17}, spread due to lithography is dominant, even in advanced CMOS technology.

2.3. ETF signal-to-noise ratio

For values of r that correspond to small (∼0.5 °C) temperature sensing errors, ϕ_{ETF} is well-defined, but the ETF's output signal V_{ETF} is quite small. For a heater power dissipation (P_{heat}) of 2.5 mW and a thermopile sensitivity of 10 mV/K, V_{ETF} is typically only 400 μV$_{pp}$. The thermopile's own Johnson noise then limits the ETF's SNR and dictates a narrow readout bandwidth. For P_{heat} = 1 mW, a bulk CMOS ETF read out at a 1S/s conversion rate has a Johnson noise-limited noise level of 0.1875 °C$_{rms}$ [4]. One reason for this poor SNR is that

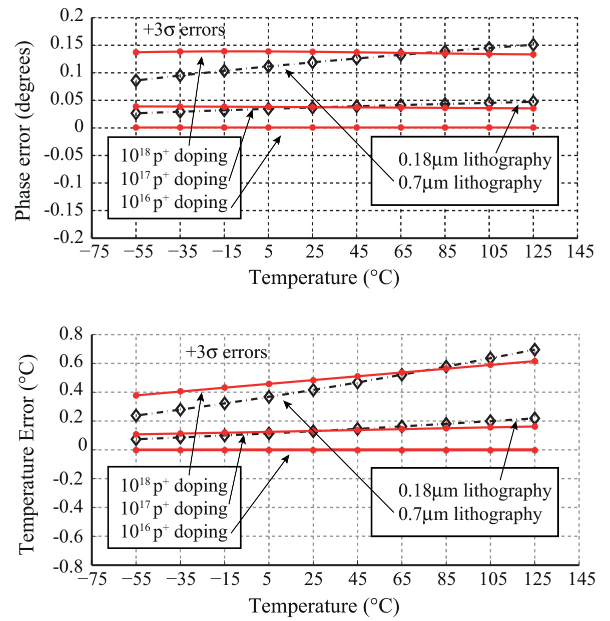

Fig. 4. Simulated phase and temperature errors due to spread in doping and lithography. All lines are 3σ limits based on statistical simulations with $N = 100$.

the thermal conductivity of silicon is rather high; another reason is that, in bulk CMOS, a substantial amount of heat is lost to the substrate, and thus does not contribute to temperature fluctuations at the surface (i.e. at the thermopile).

Because SiO_2 has a thermal conductivity 100× lower than that of silicon, it should be possible to use the buried SiO_2 (BOX) layer in an SOI process to reduce the heat loss to the substrate, thereby increasing V_{ETF}. Since there is a linear relationship between the amplitude of V_{ETF} and P_{heat}, this means that P_{heat} could be reduced proportionally. To test this hypothesis, the ETF was implemented in a partially depleted 0.5 μm SOI BiCMOS process with a thick BOX layer, buried several microns below the surface.

2.4. Modeling the effect of the SOI buried oxide layer

The effect of the BOX layer on ϕ_{ETF} can be incorporated in the model described by Eq. (4). In developing this model for bulk CMOS ETFs, the IC surface was modeled as an ideal thermal insulator. The resulting boundary condition of zero heat flow through the chip's surface was modeled by adding a mirror image heater to the model [11], as shown in Fig. 5. Using a method also used to model self-heating in SOI BJTs [13], the effect of the BOX layer can be incorporated by mirroring the heater an infinite number of times. In practice, since the magnitude of Z_{th} rapidly falls off for increasing r, only mirror image heaters with $\sim r_{,eff} < 2r_1$ contribute significantly.

Fig. 6 shows the simulated offset as a function of the BOX layer depth; $\phi_{ETF,SOI}$ clearly adds a positive offset to $\phi_{ETF,BULK}$. The upper curve in Fig. 3 is the predicted ETF transfer characteristic in this technology. Although this is in line with measurements (see Section 4), the analytical model overestimates the signal amplitude and does not include the effects of spread in BOX layer thickness. In practice, some heat also flows through the SiO_2 layers; however, taking this into account makes analytical modeling prohibitively complex. Moreover, the underlying assumption that heat diffuses through a semi-infinite medium no longer holds. Finite element simulations are more accurate, but require much more computational effort; basic FEM simulations indicate that V_{ETF} increases by ∼5.5× [14]. Further work is required to develop accurate analytical models for ETFs in SOI.

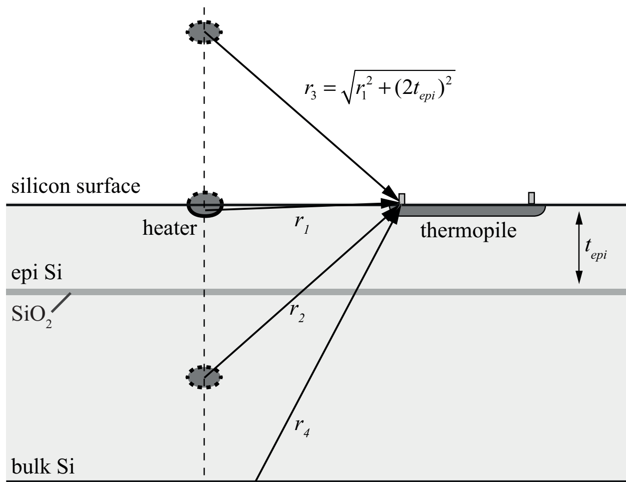

Fig. 5. Modeling technique to include the effect of a buried oxide layer on ϕ_{ETF}.

2.5. Fully depleted SOI

The analysis above has focused on the thermal properties of partially depleted SOI BiCMOS technology with relatively thick-epi layers ($t_{epi} > 1$ μm); such process technology is typically used for relatively high-voltage and analog-intensive circuitry. For modern deep submicron devices, however, fully depleted SOI (FD-SOI) technology is more common; FD-SOI technology typically uses a top silicon layer with a thickness of only tens of nanometers, while the BOX layer is typically ∼100 nm thick. By fully depleting the channel, superior electrical transistor characteristics can be achieved.

ETFs in FD-SOI technology should have an even further increase in their output signal amplitude, because the effective thermal resistance increases with reducing epi-layer thickness [15]. Moreover, such ETFs can leverage the greatly reduced lithographic inaccuracy to reduce r (keeping $\delta r/r$ constant), further improving SNR [7]. Finally, for very thin heat channels, phonon-boundary scattering will significantly reduce k [16], which also leads to an increase in amplitude (viz. through Eq. (1)). Overall, an SNR improvement of several orders of magnitude can be expected. However, it is still unknown whether spread in phonon-boundary scattering may introduce significant device-to-device temperature-sensing errors.

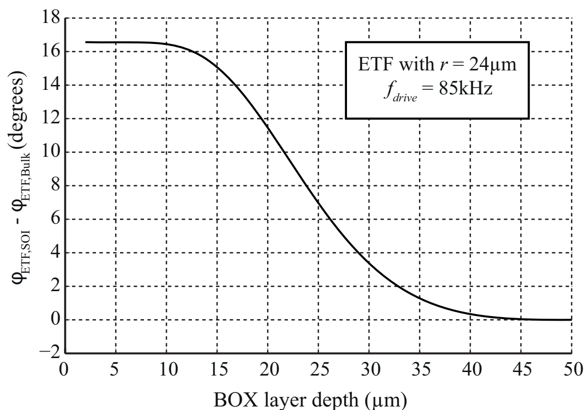

Fig. 6. Additional phase shift as a function of BOX layer depth.

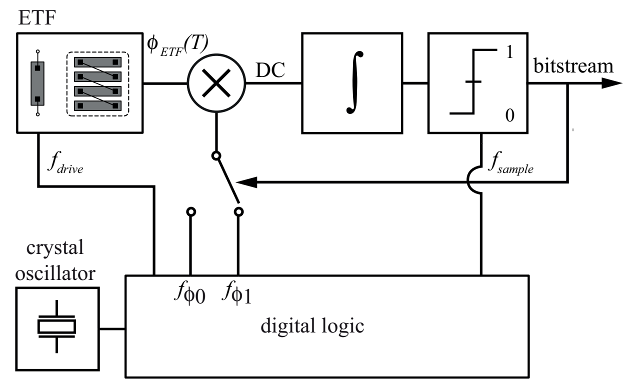

Fig. 7. Block diagram of a phase-domain sigma-delta modulator (PDΣΔM) digitizing ϕ_{ETF}.

2.6. Summary

This section has described ETF design and modeling in both bulk CMOS and SOI technology. It has shown that the accuracy of ϕ_{ETF} is a function of lithographic spread and, to lesser extent, of doping variations. Although the typical SNR of an ETF is quite low, using a buried oxide layer is expected to improve this significantly. The next section will discuss a precision readout architecture that digitizes ϕ_{ETF}.

3. Readout architecture

As discussed before, the ETF outputs a small phase-shifted signal at a known frequency, so its readout circuit should be a phase detector. Furthermore, a narrow bandwidth is required to filter the Johnson noise; this suggests the use of lock-in techniques. A narrowband phase digitizer can be realized using a phase-domain sigma-delta modulator (PDΣΔM). Temperature digitization typically requires a resolution of ∼13–14 bits: a resolution of 0.02 °C over the military temperature range (−55 °C to 125 °C) corresponds to 13.1 bits. Sigma-delta modulators can easily achieve such levels of resolution; a block diagram of a first-order, single-bit PDΣΔM is shown in Fig. 7.

The ETF is driven using a constant frequency f_{drive}, so that ϕ_{ETF} is temperature dependent. The f_{drive} signal can be derived from a crystal oscillator, which then also acts as the time reference required to convert the thermal delay to a (unitless) digital representation of temperature. The PDΣΔM's phase-differencing node is implemented by multiplying the phase-shifted output signal of the ETF is with one of two feedback signals, which are phase-shifted copies of f_{drive} having digitally generated phase shifts ϕ_0 and ϕ_1. The DC component of the resulting output is proportional to the cosine of the phase difference and equals zero when this difference is 90°. The PDΣΔM forces the average multiplier output to zero, in which case the bitstream represents a weighted average of two reference phase shifts (ϕ_0, ϕ_1) that approximates ($\phi_{ETF} - 90°$). The bitstream is then processed by a decimation filter (not shown), which limits the bandwidth and outputs a high-resolution digital output.

A 16 MHz crystal oscillator was used to drive an FPGA that generates f_{drive} (=85 kHz) and other timing signals. Based on the simulated ϕ_{ETF} for this f_{drive} (Fig. 3), the phase feedback signals ϕ_0 and ϕ_1 were set to define a ϕ_{ETF} input range from 45° to 135°. The sampling frequency f_{sample} was set to $f_{drive}/4 = 21.33$ kHz, and the bitstream was decimated using a sinc[1] decimation filter. For typical settings, the quantization noise of the PDΣΔM is much smaller than the ETF's thermal noise.

The PDΣΔM is implemented by the circuit shown in Fig. 8. Here, the integrator has been implemented by a g_m-C stage, and

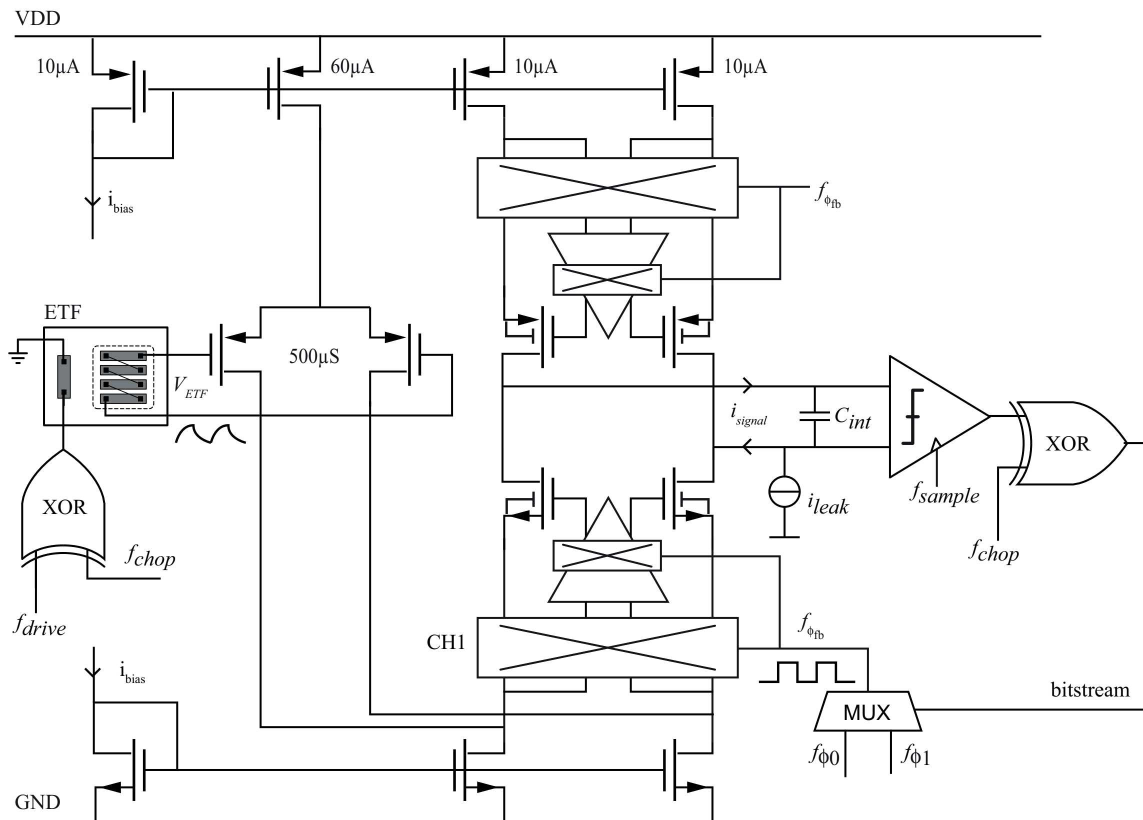

Fig. 8. PDΣΔM implementation.

the quantizer is a basic sampled comparator. The ETF output voltage, V_{ETF}, is converted to a current by a differential pair with a nominal transconductance of 500 μS. This current flows into the folding node of the g_m-stage and is demodulated by chopper CH1, which is located at the source terminals of a regulated cascode as in [4]. The demodulated output current, i_{signal}, flows into integrator C_{int} (=40pF), and the DC component of i_{signal} is proportional to $V_{ETF} \times g_m \times \cos(\phi_{ETF} - \phi_{fb})$. The comparator drives the PDΣΔM's negative feedback loop to ensure that the average current into C_{int} is zero and that the voltage swing on C_{int} is limited.

The PDΣΔM is designed so that its contributions to measurement error are small. The noise floor of the system is dominated by white noise from the thermopile. The 1/*f* noise corner of the g_m-stage is located below f_{drive}, at around 50 kHz, and the white noise contributions of the circuit are about 2× smaller than those of the ETF. The g_m-stage offset is modulated to f_{drive} by CH1 and subsequently filtered out by the integrator, so that it does not contribute error. Mismatch between the charges injected by the devices that form CH1 contributes an effective DC current that is not chopped; to reduce the effect of this current, a pair of low-frequency digital choppers was added. These choppers operate at $f_{chop} = f_{drive}/16{,}384$ and switch only once per conversion; this inverts the heat polarity, effectively inverting the polarity of any residual DC errors so that, after averaging in the decimation filter, these errors are cancelled.

Current source i_{leak} models the error current due to junction leakage. At very high temperatures, the reverse-biased junctions associated with all diffusions start to conduct significant leakage current [17]; if not reduced, this can cause temperature-sensing errors in the order of several degrees. Since this circuit was implemented in SOI, each device could have its body connected to its source terminal, so that source-body leakage is not present and drain-body leakage only manifests itself as a small current source in parallel with the device, thus only causing a small biasing error. Additionally, all sources of leakage before CH1 are modulated to AC by the chopper and subsequently filtered by C_{int}. The NMOS devices in CH1, however, have their body connected to ground to ensure a high off-resistance, so the drain-body junctions of CH1 are the dominant source of leakage. However, the low-frequency choppers also invert the effective polarity of this error, so that, over one conversion, its error contribution is cancelled.

PDΣΔMs have previously been successfully implemented in 0.7 μm and 0.18 μm bulk CMOS technologies [4,7], and their implementation in SOI technology (either partially or fully depleted) is relatively straightforward, because they are fully CMOS-compatible and do not rely on precision analog process options. Circuit simulations show that the PDΣΔM is nearly transparent: its worst-case residual error is about 0.05 °C, even at high (225 °C) temperatures. The measurement results can therefore be directly related to ETF characteristics.

4. Results

4.1. Implementation

The ETF and the PDΣΔM were fabricated in a 0.5 μm SOI BiCMOS process (Fig. 9). The device has an area of 1 mm^2, which is limited by the need for several test bondpads; an ETF occupies only about 0.01 mm^2. The ETFs are realized in a large silicon well with typical (low) epi-layer doping. The devices were packaged in ceramic DIL16 packages. The PDΣΔM consumes 2.5 mW from a 5 V supply and P_{heat} was regulated by an external voltage source and could be controlled from 0 to 7.5 mW.

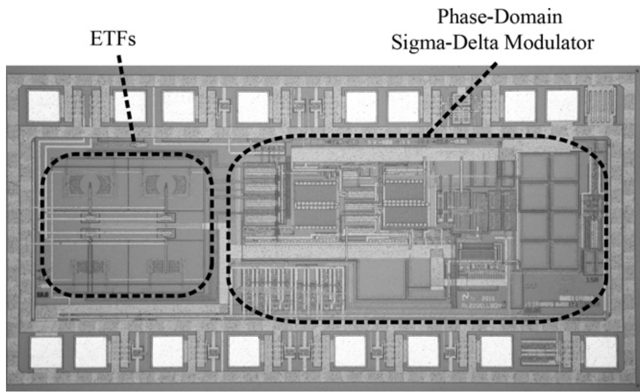

Fig. 9. Chip photo.

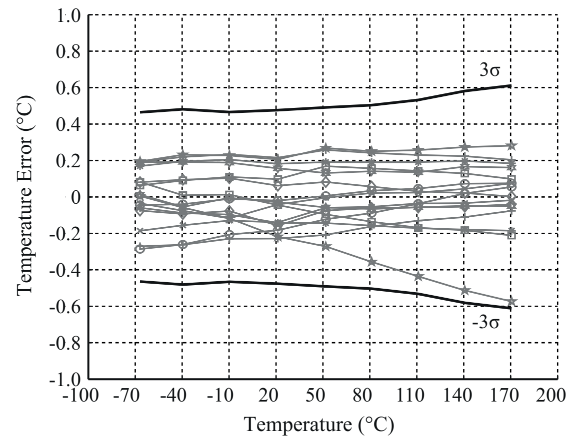

Fig. 11. Device-to-device temperature errors. The black lines indicate 3σ limits.

4.2. Measurement setup

In order to measure ϕ_{ETF} as a function of temperature, the devices were mounted in good thermal contact with a large aluminum block, of which the temperature was swept. A Pt100 thermistor, calibrated to 10 mK inaccuracy at the Dutch Metrology Institute, was placed inside the aluminum block to be used as the reference temperature sensor. Over the −70 °C to 170 °C range, the devices were characterized using a Vötsch VTM7004 climate chamber.

4.3. Device characteristics

By sweeping temperature and comparing the measured ϕ_{ETF} of many devices to the temperature reading from the reference thermistor, a master curve that maps the digital output to absolute temperature can be calculated. Fig. 10 shows this master curve, based on 16 devices from a single batch. It can be seen that, as expected, ϕ_{ETF} is approximately proportional to $T^{0.9}$. When compared, however, to the same ETF geometry in bulk CMOS [4], ϕ_{ETF} has a clear positive offset, which is due to the effect of the buried thermally insulating layer, as was modeled in Section 2. The value of this offset is about 8°, which is about half of the ∼16° predicted by Fig. 3. This is likely due to the fact that, unlike in the model, the BOX layer is not a perfect thermal insulator.

The output of each device was compared to the master curve so that the device-to-device errors could be calculated. Fig. 11 shows the *untrimmed* device-to-device spread for 16 devices from a single batch, indicating a worst-case temperature-sensing inaccuracy of ±0.6 °C (3σ) over the −70 °C to 170 °C temperature range. This spread is in line with earlier results at a similar lithographic node in bulk CMOS [4], and these results show that the ETF indeed has a low untrimmed inaccuracy over a wide temperature range. At lower temperatures, the spread is slightly higher than expected from modeling; this is likely due to minor influence from the spread in the properties of the BOX layer. Fig. 11 also shows that the devices do not suffer from leakage at high temperatures.

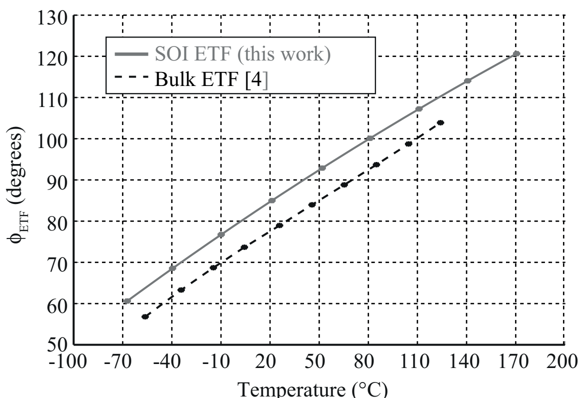

Fig. 10. Measured ϕ_{ETF} as a function of temperature, compared to an ETF in bulk CMOS.

4.4. Signal-to-noise ratio

To measure SNR, temperature was kept constant and ϕ_{ETF} was digitized at a conversion rate of 1 Hz. At P_{heat} = 1 mW, the quantization noise of the PD$\Sigma\Delta$M can be neglected and the system is thermal-noise limited. The measured noise level was 0.037 °C$_{rms}$ (based on 200 conversions), which is a 5× improvement over the same ETF in bulk CMOS [4]. A second ETF had 2× more thermocouples, which was achieved by reducing the thermocouple pitch and by fully surrounding the heater with thermocouples, completing the phase contour illustrated in Fig. 2. Capacitive coupling between the heater and the thermopile was prevented by metal shielding. This ETF achieved a noise floor of 0.026 °C$_{rms}$, representing a further 1.4× improvement.

This 7× SNR improvement demonstrates the feasibility of wide-range thermal diffusivity sensors with sub-mW power dissipation. In SOI processes with higher lithographic accuracy, the ETF's dimensions could be reduced [7] to further improve the signal to noise ratio.

4.5. Batch-to-batch variations

According to the theory presented in Section 2, the device-to-device spread of ETFs should be mainly defined by lithographic spread. This means that, ideally, batch-to-batch variations (e.g. in doping concentration and layer thickness) should only have a minor effect on the ETF characteristics. To test this, the same ETF layout was fabricated on 3 process runs over a 1-year period. Since these were multi-project wafer ("MPW") runs, this also tests for maskset to maskset variations. Variations in BOX layer depth were not tracked during fabrication and have not been measured. Fig. 12 shows the device-to-device spread of 32 devices from 3 batches and the corresponding batch averages. The 3σ error bounds are at about ±0.6 °C and variation in batch averages is in the order of ±0.1 °C, demonstrating that the effect of batch-to-batch variations is limited.

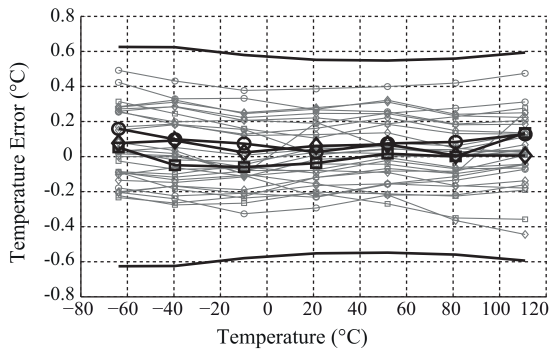

Fig. 12. Device-to-device spread for 32 devices from different fabrication lots. The middle bold lines are lot averages.

4.6. Doping sensitivity

Since ETFs are *thermal* rather than *electrical* devices, they are much less sensitive to spread in doping concentration. As was discussed in Section 2, doping only contributes significant errors at high doping levels. This is in agreement with earlier work [5] that has shown that that the thermal diffusivities of p-doped silicon ($N_a = 5 \times 10^{14}/\text{cm}^3$) and n$^+$-doped silicon ($N_d = 3 \times 10^{16}/\text{cm}^3$) were equal to within 0.1%. At these relatively low doping levels, however, it is notoriously difficult to measure associated changes in k at 'high' ($T > 200$ K) temperatures, since phonon–phonon scattering has much higher scattering rates than phonon-impurity scattering [9].

In this work, a second experiment was performed using an n^{++}-implant, normally used to reduce the resistivity of a silicon well (Fig. 13a); its doping concentration is more than 2 orders of magnitude higher than in [5]. This high doping level leads to a measureable increase in ϕ_{ETF} of ~2.3°, corresponding to ~9 °C (Fig. 13b). Device-to-device spread on a single wafer did not increase significantly, but in contrast to the regular ETF, this ETF was found to have significant batch-to-batch errors (~0.8 °C shifts in average), which can clearly be attributed to the spread in doping concentration. Since typical doping concentrations are more than 2 orders of magnitude lower, this reaffirms that for regular ETFs, the effect of doping is very small.

4.7. Self-heating

Since ETFs dissipate heat to measure temperature, there is an intrinsic tradeoff between power consumption and temperature-sensing accuracy. The total power consumption ($P_{total} = P_{heat} + P_{circuit}$) heats the die above ambient through the finite thermal resistance of the package. Additionally, power dissipated by the ETF locally increases the die temperature, which locally influences D.

To determine R_{th}, ambient temperature was kept constant while the ETF was driven at high power levels. P_{heat} was ramped from 2.5 to 7 mW in several steps, and the measured ϕ_{ETF} was converted to temperature through Fig. 10 master curve. Fig. 14 shows the result for 4 devices; the self-heating causes a significant temperature offset (about 0.7 °C for $P_{total} = 3.5$ mW) and the extrapolated R_{th} is about 250 K/W. This is significantly higher than for bulk CMOS (~50–100 K/W) due to the presence of the BOX layer, and this is in good agreement with the 5× increase in V_{ETF} discussed in Section 4.4.

However, for a certain ETF geometry, all ETFs will self-heat in roughly the same way, so that only the spread in self-heating (due to either spread in R_{th} or P_{heat}) will cause device-to-device temperature errors; the nominal component will be included in the

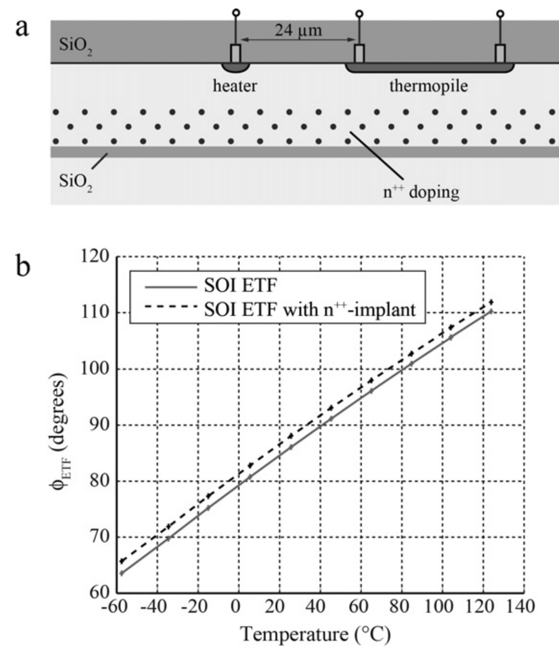

Fig. 13. ETF with highly doped buried layer and measured phase characteristics.

master curve that maps the digital output to temperature (see Section 4.3). The device-to-device spread in R_{th} is only about ±2%, so that at a typical power levels ($P_{heat} = 1$ mW), spread in self-heating corresponds to only ±5 mK errors.

For ETFs with reduced r, or for ETFs implemented in SOI technology with a very thin top silicon layer (FD-SOI), it is expected that R_{th} will increase further, so that self-heating will increase accordingly. However, the DC and AC thermal impedance of an ETF are coupled (viz. through Eq. (1)), so the ETF's SNR will have increased proportionally, allowing lower P_{heat} for the same resolution. If a higher resolution (or shorter conversion time) is required, P_{heat} should not be reduced, in which case spread in self-heating could eventually increase the ETF's temperature-sensing errors.

4.8. Power supply rejection

All integrated temperature sensors have finite power supply rejection ratio (PSRR), which means that small variations in V_{DD} are erroneously interpreted as temperature changes. For temperature sensors based on BJTs, this is typically in the order of 0.1 °C/V [18],

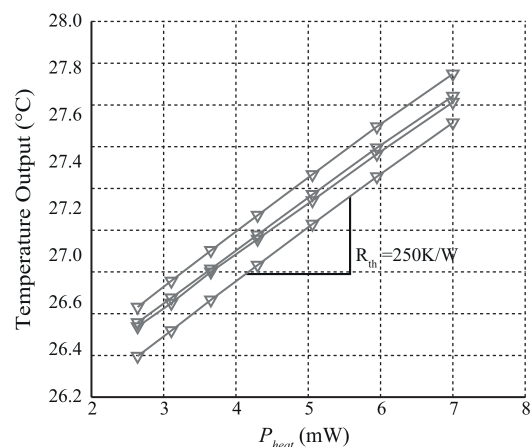

Fig. 14. Measured self-heating as a function of ETF heater power (based on 4 devices).

Table 1
Comparison between high-temperature BJT-based temperature sensors and ETFs.

	ADT7312 [2]	LM95172 [3]	Bulk CMOS ETF[6]	SOI ETF (this work)
Worst-case inaccuracy	±1.0 °C trimmed	±3.0 °C trimmed	±0.7 °C (3σ) untrimmed	±0.6 °C (3σ) untrimmed
Temperature range	−55 °C to 175 °C	−40 °C–200 °C	−70 °C–160 °C	−70 °C–225 °C
Power dissipation	0.73 mW	1.2 mW	3.5 mW	3.5 mW
Conversion rate	4.16S/s	2.8S/s	1S/s	1S/s
Resolution	0.0078 °C	0.0078 °C	0.1875 °C$_{rms}$	0.026 °C$_{rms}$

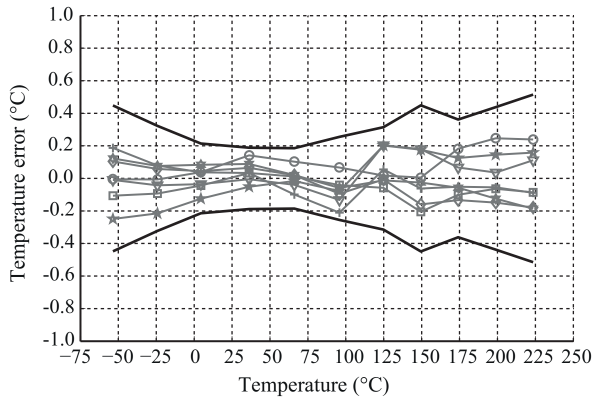

Fig. 15. Device-to-device temperature errors over a wide temperature range.

but it can be as small as 0.03 °C/V [19]. In ETF-based temperature sensors, two sources of finite PSRR can be identified: changes in the amplitude of the square wave applied to the heater, and errors in the PDΣΔM. The latter is very small, since the PDΣΔM is fully differential and processes a time-domain input signal. The supply voltage of the PDΣΔM was swept from 4.5 to 5.5 V, but no variation in ϕ_{ETF} could be measured. A more dominant source of finite power supply rejection comes from changes in V_{heat}, and therefore in P_{heat}. In this chip, V_{heat} is set by an external voltage source, connected to the heater through a separate pin, so variations in P_{heat} are proportional to $V_{heat}{}^2$. Through R_{th} (∼250 K/W), variations in V_{heat} cause variations in self-heating; the resulting change in temperature is given by:

$$\Delta T = P_{heat}R_{th} = \frac{V_{heat}^2 R_{th}}{2R_{heater}} \rightarrow \frac{\partial T}{\partial V_{heat}} = \frac{V_{heat}R_{th}}{R_{heater}} \quad (7)$$

In the current system, spread in V_{heat} introduces a finite PSRR of about 0.16 °C/V at P_{heat} = 1 mW. This sensitivity can V_{heat} can be reduced by decoupling P_{heat} from V_{heat}, e.g. by using a constant-power control circuit in which a feedback loop keeps $I_{heat} \times V_{heat}$ equal to a constant value.

4.9. Very high temperature operation

In an additional high-temperature experiment, a Carbolite HT-5/28 high-temperature oven was used to measure from 125 °C to 225 °C, while the climate chamber was used for lower temperatures. To obtain reliable data at very high temperatures, Teflon wiring and high-temperature solder were used to connect to the devices. As can be seen from Fig. 15, ETFs also work at temperatures as high as 225 °C, while maintaining an untrimmed inaccuracy of ±0.5 °C (3σ).

4.10. Comparison to BJT-based sensors

Based on the results described above, ETF-based temperature sensors can be compared to conventional temperature sensors based on bipolar transistors. Although state-of-the art BJT-based temperature sensors [18] consume much less power than the ETF-based sensors in this work (7.5 μW vs. 3.5 mW), ETFs have two important advantages: firstly, they operate over a wide temperature range and are unaffected by leakage currents; secondly, their untrimmed inaccuracy is as low as ±0.6 °C (3σ) over this range. Table 1 shows a comparison between two commercially available high-temperature sensors and ETFs; several key temperature sensor specifications are listed.

5. Conclusions

This paper has discussed the modeling, design and measurement of temperature sensors based on thermal diffusivity sensing in SOI technology. Such sensors use an Electrothermal Filter to measure the temperature-dependent time it takes for heat to diffuse through a silicon chip. For ETFs in bulk CMOS, a significant amount of heat is lost to the substrate. However, in an SOI process the presence of a buried SiO_2 layer reduces this heat loss, leading to up to 7× lower power consumption compared to ETFs in bulk CMOS.

Sensors from a single wafer have an *untrimmed* device-to-device spread of ±0.6 °C (3σ) from −70 °C to 225 °C, while the effects of wafer-to-wafer and batch-to-batch variations were measured to be at the 0.1 °C level. Thermal diffusivity sensors therefore do not require any kind of trimming to achieve <1.0 °C inaccuracy, which is the best performance reported for integrated temperature sensors. The effects of spread in doping concentration are very small and well-understood.

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References

[1] A.L. Aita, M.A.P. Pertijs, K.A.A. Makinwa, J.H. Huijsing, A CMOS smart temperature sensor with a batch-calibrated inaccuracy of ±0.25 °C (3σ) from −70 °C to 130 °C, IEEE ISSCC Dig. Tech. Papers (February) (2009) 342–343.
[2] ADT7312 specifications, Analog Devices, available online through http://www.analog.com.
[3] [95172LM] specifications, National Semiconductor, available online through http://www.national.com.
[4] S.M. Kashmiri, S. Xia, K.A.A. Makinwa, A temperature-to-digital converter based on an optimized Electrothermal Filter, IEEE J. Solid State Circuits (July) (2009) 2026–2035.
[5] C. Zhang, K.A.A. Makinwa, The effect of substrate doping on the behaviour of a CMOS electrothermal frequency-locked-loop, Dig. Transducers 2007 (June) (2007) 2283–2286.
[6] C.P.L. van Vroonhoven, K.A.A. Makinwa, Thermal diffusivity sensors for wide-range temperature sensing, Proc. IEEE Sensors 2008 (October) (2008) 764–767.
[7] C.P.L. van Vroonhoven, D. D'Aquino, K.A.A. Makinwa, A Thermal-diffusivity-based temperature sensor with an untrimmed inaccuracy of ±0.2 °C (3σ) from −55 °C to 125 °C, IEEE ISSCC Dig. Tech. Papers (February) (2010) 314–315.
[8] K. Kasten, et al., Capacitive pressure sensor with monolithically integrated CMOS readout circuit for high temperature applications, Sens. Actuators A: Phys. 97–98 (April) (2002) 83–87.
[9] R. Berman, Thermal Conduction in Solids, Oxford University Press, 1976.

[10] M. Asheghi, et al., Thermal conduction in doped single-crystal silicon films, J. Appl. Phys. 91 (April) (2002) 5079–5088.
[11] T. Veijola, Simple model for thermal spreading impedance, Proc. BEC' 96 (October) (2005) 73–76.
[12] S. Xia, K.A.A. Makinwa, Design of an optimized Electrothermal Filter for a temperature-to-frequency converter, Proc. IEEE Sensors 2007 (October) (2007) 1255–1258.
[13] A. Pacelli, P. Palestri, M. Mastrapasqua, Compact modeling of thermal resistance in bipolar transistors on bulk and SOI substrates, IEEE Trans. Electron Devices 49 (June (6)) (2002) 1027–1033.
[14] S. Xia, Modeling and Optimization of an Electrothermal Filter, M.Sc. Thesis, Delft University of Technology, Delft, The Netherlands, July 2007.
[15] L.T. Su, et al., Measurement and modeling of self-heating in SOI NMOSFET's, IEEE Trans. Electron Devices 41 (January (1)) (1994) 69–75.
[16] M. Asheghi, et al., Temperature-dependent thermal conductivity of single-crystal silicon layers in SOI substrates, Trans. ASME 120 (February) (1998) 30–36.
[17] P.C. de Jong, G.C.M. Meijer, A.H.M. van Roermund, A 300 °C dynamic-feedback instrumentation amplifier, IEEE J. Solid State Circuits 33 (December) (1998) 1999–2009.
[18] K. Souri, K.A.A. Makinwa, A 0.12 mm2 7.5 μW micropower temperature sensor with an inaccuracy of ±0.2 °C (3σ) from –30 °C to 125 °C, IEEE J. Solid State Circuits 46 (July (7)) (2011) 1693–1700.
[19] M.A.P. Pertijs, K.A.A. Makinwa, J.H. Huijsing, A CMOS temperature sensor with a 3σ inaccuracy of ±0.1 °C from −55 °C to 125 °C, IEEE J. Solid State Circuits 40 (December (12)) (2005) 2805–2815.
[20] C.P.L. van Vroonhoven, K.A.A. Makinwa, An SOI thermal-diffusivity-based temperature sensor with ±0.6 °C (3σ) untrimmed inaccuracy from −70 °C to 170 °C, Dig. Transducers 2011 (June) (2011) 2887–2890.

Biographies

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